PAT-NO: JP02001166744A

DOCUMENT-IDENTIFIER: **JP 2001166744 A**

TITLE: DRIVING CIRCUIT FOR ELECTRO-OPTICAL DEVICE, DATA LINE DRIVING CIRCUIT, SCANNING LINE DRIVING CIRCUIT, ELECTRO-OPTICAL DEVICE, AND ELECTRONIC EQUIPMENT

PUBN-DATE: June 22, 2001

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APPL-NO: JP11347657

APPL-DATE: December 7, 1999

INT-CL (IPC): G09G003/36, G02F001/133 , G09G003/20

ABSTRACT:

PROBLEM TO BE SOLVED: To prevent overlapping periods of output signals of data line driving circuits and scanning line driving circuits from occurring without using external signals.

SOLUTION: For example, plural latch circuits 1430 sequentially shift transfer start pulses DX according to clock signals CLX and reversed clock signals CLXINV and output them. In this case, an active period of an output signal of each **NAND** circuit 1464 arranged correspondingly between two successive unit circuits 1430 is limited by a signal delayed by td from a signal outputted from the latter stage unit circuit 1430 of the

successive two
unit circuits (each **NOR** circuit 1474).

* NOTICES *

Same Assignee inventor
But 102(b) pub on June 2001

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the electro-optic device in which a high-definition display is possible, its drive circuit, a data-line drive circuit, a scanning-line drive circuit, and the electronic equipment that used this electro-optic device for the display.
[0002]
[Description of the Prior Art] Conventional liquid crystal equipment forms two or more data line and two or more scanning lines in an image display field, and has prepared the thin film transistor ("TFT" is called below Thin FilmTransistor:) and the pixel electrode respectively corresponding to the crossover of each data line and each scanning line. Turning on and off is controlled by the electrical potential difference of each scanning line with which TFT corresponds. And if TFT is turned on, the electrical potential difference of the data line will be impressed to a pixel electrode through TFT.
[0003] The drive circuit of liquid crystal equipment consists of a data-line drive circuit for supplying a picture signal, a scan signal, etc. to the data line, the scanning line, etc. which were wired to the image display field to predetermined timing, a scanning-line drive circuit, a sampling circuit, etc. The active element which constitutes these drive circuits is TFT of the P channel mold formed of the same process in TFT formed in an image display field, and N channel mold.
[0004] It is the circuit which a data-line drive circuit carries out the sequential shift of the transfer signal supplied to the beginning of a horizontal scanning period according to a clock signal, it is the circuit which outputs this as a sampling signal, and a scanning-line drive circuit is equipped with two or more latch circuits, carries out the sequential shift of the transfer signal supplied to the beginning of a vertical-scanning period according to a clock signal, and outputs this as a scan signal. Moreover, a sampling circuit is a circuit which is equipped with the switch for a sampling formed for every data line, samples the picture signal supplied from the outside according to the sampling signal by the data-line drive circuit, and is supplied to each data line.
[0005] Drawing 13 is the block diagram showing the configuration of the data-line drive circuit 1400 concerning the conventional technique. The data-line drive circuit 1400 consists of a latch circuit 1430 and NAND circuit 1464. Among these, a latch circuit 1430 is a circuit which outputs the input level in front of that at the time of level transition (starting falling) of a clock signal CLX and its reversal clock signal CLXINV. Since this output signal is supplied as an input signal of the latch circuit 1430 located in the next step, according to a clock signal CLX and reversal clock signal CLXINV, the sequential output of the transfer initiation pulse DX supplied to the latch circuit 1430 of the first rank is carried out from each latch circuit 1430. Moreover, each NAND circuit 1464 is respectively formed between two continuous latch circuits 1430, and the sampling signals Q1-Qn are outputted from them.
[0006]
[Problem(s) to be Solved by the Invention] By the way, the data-line drive circuit 1400 is constituted by TFT of a P channel mold and N channel mold as mentioned above. Even if the ON state current and the Vth (threshold voltage of transistor) property of TFT exist on the same substrate, variation produces

them with the substrate location. For example, although the value of Vth of TFT is adjusted by ion DOPINGU in a manufacture process, it is very difficult for making the amount of doping uniform ideally covering a large area. For this reason, in TFT formed in the distant location, Vth will be different.

[0007] thus, every which constitutes the data-line drive circuit 1400 -- the property of TFT -- the propagation delay time of a barrack, and the each NAND circuit 1464 and each latch circuit 1430 -- or the build up time of a signal -- a barrack -- it becomes things.

[0008] Here, the trouble which originates in the Vth value of the P channel mold TFT at this supposing the case where variation arises is explained concretely. Generally, when TFT constitutes a latch circuit 1430 and NAND circuit 1464, the P channel mold TFT is connected and used for a high potential side power source. For this reason, the Vth value of the P channel mold TFT will arise [variation] to the generating timing of the rising edge of the output signal of a barrack, and a latch circuit 1430 and NAND circuit 1464.

[0009] The timing chart shown in drawing 14 is shown including the wave of the output signal of a latch circuit 1430 or NAND circuit 1464 to variation. In this drawing, the field smeared away black is the variation range resulting from a rising edge.

[0010] Temporarily, if the propagation delay time of the 1st step of latch circuit 1430 is min, the output signal P1 of this latch circuit 1430 will start on H level from L level in timing t1. On the other hand, if the propagation delay time is max, an output signal P1 will start on H level from L level in timing t2. The variation in the range from timing t1 to t2 will be produced at the time of initiation of a result and the active (H level) period of this signal P1. In drawing, the period of this variation is indicated to be tb. Here, since only the variation in the Vth value of the P channel mold TFT is taken into consideration, it is timing t5 at the time of termination of the active (H level) period of an output signal P1, and variation does not exist.

[0011] Similarly, the variation in the range of t4, i.e., the period of tb, has arisen from the initiation timing t3 of the active (H level) period of the output signal P2 of this latch circuit, and the 2nd step of latch circuit 1430 serves as the termination timing t6 of an active (H level) period. Hereafter, the same is said of the latch circuit 1430 after the 3rd step.

[0012] Next, the output signal Q1 of NAND circuit 1464 installed among the 2nd step of latch circuit 1430 with the 1st step is considered. As mentioned above, variation exists in the signals P1 and P2 supplied to this NAND circuit 1464 at the time of initiation of an active (H level) period. Among these, the variation at the time of initiation of the active (H level) period of a signal P2 is producing the variation (t4 from timing t3, period tb) at the time of initiation of the active (L level) period of the output signal Q1 of this NAND circuit 1464. Moreover, variation will arise from timing t5 in the range of t6 (tb period) also at the time of the standup of a signal Q1 (at the time of termination of an active period) by the variation in the Vth value of the P channel mold TFT which constitutes this NAND circuit 1464. In addition, although the variation in the range of t6 (tb period) is produced from timing t5 all over drawing also at the time of initiation of the active (H level) period of a signal P3, it is unrelated to the variation in the above-mentioned signal Q1.

[0013] As for an active period, in the time of - termination, about the output signal Q2 of NAND circuit 1464 installed among the 3rd step of latch circuit 1430 with the 2nd step, the variation in tb period exists similarly at the time of initiation.

[0014] Here, its attention is paid at the time of termination of the active (L level) period of a signal Q1, and initiation of the active (L level) period of a signal Q2. Since both periods are in the range of timing t5 and t6 (tb period), the time of termination of the active (L level) period of a signal Q1 is timing t6, and also when the time of initiation of the active (L level) period of a signal Q2 is timing t5, it may happen. In this case, the active (L level) period of both signals will be overlapped between t6 (tb period) from timing t5. Furthermore, overlap with the same said of the signal after Q3 may occur.

[0015] When such signals Q1-Qn are used as a sampling signal, the overlap of a sampling period arises. This means that the picture signal which should be essentially sampled by a certain data line is supplied also to another data line. In this case, the same picture signal is incorporated by two or more data lines, a

result, display resolution, and a gradient deteriorate and the problem of falling display grace arises.
[0016] Especially, recently, that high-frequency-ization of a dot clock should be coped with, while carrying out serial-parallel conversion (phase expansion) of the one picture signal to two or more m lines, these m picture signals are sampled to coincidence according to a sampling signal, and the technique supplied to the m data lines is developed. In the liquid crystal equipment which applied such a technique, if a sampling signal overlaps and is outputted, since deterioration of display grace will occur per m, the problem of being easy to be detected visually arises.
[0017] As a cure against a fall of this display grace, the external input of the limit signal (enable signal) is carried out to a sampling signal, and it is also considered that this restricts the active period of a sampling signal. Although the days of supply of the picture signal to the data line are decided by the active period of a sampling signal, since parasitic capacitance accompanies the data line, it is necessary to lengthen the active period of a sampling signal as much as possible. That is, to supply a limit signal from the exterior and restrict an active period, it is necessary to make pulse width of a limit signal extent which can cancel an overlap period narrowly (about several ns). It is necessary to drive a limit signal with a high slew rate, and, for that, there is a problem that the consumed electric current of a drive circuit which drives a limit signal increases. On the other hand, since pulse width of a limit signal must be made large in order to control the consumed electric current of a drive circuit, there is a problem that a sampling signal will be restricted beyond the need (enable).
[0018] The place which this invention is made in view of the situation mentioned above, and makes into that purpose is to prevent generating of the overlap period of the sampling signal outputted from a data-line drive circuit, and the signal outputted from a scanning-line drive circuit, without using an external signal, and provide the drive circuit of the electro-optic device which raises display grace and an electro-optic device, and a list with the electronic equipment which used this electro-optic device for the display.
[0019]
[Means for Solving the Problem] If it is in the drive circuit of the electro-optic device concerning this invention in order to solve the above-mentioned technical problem It is premised on being used for the electro-optic device which has the switching element prepared corresponding to the crossover with two or more scanning lines, two or more data lines, and said each scanning line and said each data line, and a pixel electrode. Two or more unit circuits which carry out a sequential shift and output an input signal according to a clock signal, Corresponding to two continuous unit circuits, it is prepared respectively, and has two or more unit drive circuits which generate the signal which chooses said each scanning line or said each data line. Said unit drive circuit it is inputted into the delay circuit which delays a latter output signal between two corresponding unit circuits, and this unit drive circuit -- this -- it is characterized by providing the limiting circuit which restricts the active period determined by the output signal of two unit circuits based on the output signal of said delay circuit.
[0020] According to this invention, even if it is the case where the active period determined by the output signal of said two unit circuits overlaps mutually, since said active period is restricted by said limiting circuit, the period overlapped in the signal outputted from said limiting circuit does not produce it. Therefore, if this signal is used as for example, a sampling signal, since it will not be sampled by the data line with which the same picture signals differ, degradation of display grace is not produced.
[0021] Here, as for said unit drive circuit, it is desirable that it is the circuit which restricts the initiation timing of said active period based on the output signal of said delay circuit. In this case, even if it is the case where the active period determined by the output signal of said two unit circuits overlaps other things for example, it does not become that do not overlap the signal after a limit mutually, for this reason it causes degradation of display grace by it in the first half since the initiation part of this active period is restricted by the limiting circuit.
[0022] It adds, said delay circuit is constituted from an inverter, and, as for said limiting circuit, it is desirable to have the NAND circuit which inputs the output signal of two continuous unit circuits, and the NOR circuit which restricts the active signal of the output signal of this NAND circuit with the output signal of said inverter. According to this, adjustment of the time delay in a delay circuit can carry

out easily and certainly, and can also prevent the overlap of the signal outputted from a NOR circuit.
[0023] Moreover, if it is in the data-line drive circuit of the electro-optic device concerning this invention The switching element connected to the scanning line, two or more data lines, and two or more of said each scanning line and said each data line, Two or more unit circuits which carry out a sequential shift and output an input signal according to a clock signal on the assumption that it is used for the electro-optic device which has the pixel electrode connected to said switching element, Two or more unit drive circuits which generate the sampling signal which is respectively established corresponding to two continuous unit circuits, and chooses said each data line, It has two or more switches which sample a picture signal based on said sampling signal, and are supplied to said data line. Said unit drive circuit The delay circuit which delays a latter output signal between two corresponding unit circuits, it is inputted into this unit drive circuit -- this -- it may be characterized by providing the limiting circuit which restricts the active period determined by the output signal of two unit circuits based on the output signal of said delay circuit.
[0024] Degradation of display grace is not produced without supplying the data line with which the same picture signals differ, if this signal is used as a sampling signal since the period overlapped mutually does not produce the signal outputted from the above-mentioned limiting circuit according to this.
[0025] Moreover, in this invention, it is desirable that it is the thing which two or more switches corresponding to said each data line are blocked [thing] corresponding to said data line of m (m is the two or more natural numbers) book, and had said sampling signal blocked and to supply for every switch.
[0026] High-frequency-ization of a dot clock can be coped with without raising the engine performance of the switch which samples a picture signal according to this.
[0027] Moreover, if it is in the scanning-line line drive circuit of the electro-optic device concerning this invention It is premised on being used for the electro-optic device which has the switching element prepared corresponding to the crossover with two or more scanning lines, two or more data lines, and said each scanning line and said each data line, and a pixel electrode. Two or more unit circuits which carry out a sequential shift and output an input signal according to a clock signal, Corresponding to two continuous unit circuits, it is prepared respectively, and has two or more unit drive circuits which generate the signal which chooses said each scanning line. Said unit drive circuit The delay circuit which delays a latter output signal between two corresponding unit circuits, it is inputted into this unit drive circuit -- this -- it may be characterized by providing the limiting circuit which restricts the active period determined by the output signal of two unit circuits based on the output signal of said delay circuit.
[0028] Degradation of display grace is not produced without supplying the scanning line with which the same picture signals differ, if this signal is used as a scanning-line signal since the period overlapped mutually does not produce the signal outputted from the above-mentioned limiting circuit according to this.
[0029] Moreover, if it is in the electro-optic device concerning this invention, it has the drive circuit and image display field of the above-mentioned electro-optic device, and as for said image display field, it is desirable to consist of substrates of the pair which carries out phase opposite, and to equip one substrate with the transistor opened and closed according to the scan signal supplied to said scanning line, while being inserted between the pixel electrode arranged in the shape of a matrix, said pixel electrode, and said data line. An ON pixel and an off pixel become disengageable electrically with this transistor, and the good highly minute display of the contrast of image quality is attained.
[0030] Moreover, if it is in the electrical machinery and apparatus concerning this invention in order to solve the above-mentioned technical problem, since it is characterized by using the above-mentioned electro-optic device for a display, it becomes possible to perform a high-definition display.
[0031]
[Embodiment of the Invention] Hereafter, it explains, referring to a drawing about the operation gestalt of this invention. Hereafter, it explains as an electro-optic device concerning this operation gestalt by

making into an example the liquid crystal equipment using the liquid crystal which is an opto electronics material.

[0032] <Liquid crystal equipment whole configuration> drawing 1 shows the block diagram showing the electric configuration of this liquid crystal equipment. Liquid crystal equipment consists of a liquid crystal panel 100, a timing generator 200, and a picture signal processing circuit 300. A timing generator 200 is equipment which outputs the control signal (it mentions later if needed.) used in each part of this liquid crystal equipment.

[0033] The S/P conversion circuit 302 in the picture signal processing circuit 300 is a circuit which carries out serial-parallel conversion of the one picture signal Video at six picture signals. The reason for carrying out serial-parallel conversion of the input picture signal Video at six lines is for lengthening impression time amount of the picture signal to the source field of TFT which constitutes the switch 151 for a sampling, and fully securing the sampling time and charge and discharge time in a sampling circuit 150.

[0034] Magnification and an inverter circuit 304 are circuits which are made to reverse that for which reversal is needed among the picture signals by which serial-parallel conversion was carried out, amplify suitably after this, and are supplied in juxtaposition to a liquid crystal panel 100 as picture signals VID1-VID6. In addition, whether the impression methods of a data signal of whether it is the need are the polarity reversals of ** scanning-line 112 unit, reversal is the polarity reversals of ** data-line 114 unit, or they are the polarity reversals of ** pixel unit and the polarity reversals of ** screen unit respond, it is set, and the reversal period is set as 1 horizontal-scanning period, 1 vertical-scanning period, or a dot clock period.

[0035] <The configuration of a liquid crystal panel>, next the electric configuration of a liquid crystal panel 100 are explained. The liquid crystal panel 100 has the composition that the component substrate and the opposite substrate countered and each other were stuck in the electrode forming face. In drawing 1 , two or more scanning lines 112 are formed in a component substrate in parallel along the direction of X, and two or more data lines 114 are formed in it in parallel along the direction of Y. And while the gate electrode of TFT116 which serves as a switch for controlling each pixel at each intersection of this scanning line 112 and the data line 114 is connected to the scanning line 112 and the source electrode of TFT116 is connected to the data line 114, the drain electrode of TFT116 is connected to the pixel electrode 118. Each pixel is constituted by the pixel electrode 118, the common electrode formed in the opposite substrate, and the liquid crystal pinched among these two electrodes, and is arranged in the shape of a matrix corresponding to each intersection of the scanning line 112 and the data line 114.

[0036] The drive circuit 120 consists of a scanning-line drive circuit 130, a data-line drive circuit 140, and a sampling circuit 150, is in the opposed face of the component substrate which consists of glass which has permeability and insulation, and is formed in the periphery of a viewing area.

[0037] <The configuration of a data-line drive circuit>, next the data-line drive circuit 140 concerning this operation gestalt are explained. The data-line drive circuit 140 outputs the sampling signals S1-Sn in predetermined sequence by carrying out the sequential shift of the transfer initiation pulse DX supplied to the beginning of a horizontal scanning period according to a clock signal CLX and its reversal clock signal CLXINV.

[0038] Drawing 2 is the block diagram showing the configuration of the data-line drive circuit 140. As shown in this drawing, the profile configuration of the data-line drive circuit 140 is carried out from the latch circuit 1430 and n logical circuit units U1-Un by which cascade connection was carried out to the stage (n+1). In addition, a clock signal CLX, its reversal clock signal CLXINV, and the transfer initiation pulse DX are supplied by each with the timing generator 200 in drawing 1 synchronizing with picture signals VID1-VID6.

[0039] (n+1) The latch circuit 1430 connected to the stage functions as a shift register. One latch circuit 1430 supplies the output signal as an input signal of the latch circuit 1430 located in the latter part while outputting the input signal level in front of that at the time of level transition (falling and starting) of the clock signal CLX supplied and its reversal clock signal CLXINV.

[0040] Drawing 3 shows an example of the concrete configuration of a latch circuit 1430. A latch circuit

1430 is constituted by clocked inverters 1432 and 1436 and the inverter 1434, and these consist of a P channel mold TFT and an N channel mold TFT further. Hereafter, each configuration about the latch circuit 1430 of odd level (the i-th step) and the latch circuit 1430 of even level (the i+1st step) is described.

[0041] The clocked inverter 1432 of odd level holds this condition to the standup of the following clock signal CLX while reversing the input signal in the standup (falling of reversal clock signal CLXINV) of a clock signal CLX. The clocked inverter 1436 of this stage holds this condition to the standup of the next clock signal CLXINV while reversing the input signal in the standup (falling of a clock signal CLX) of reversal clock signal CLXINV. The clocked inverters 1432 and 1436 of even level correspond to that to which the relation between the clock signal CLX inputted and reversal clock signal CLXINV replaced the thing of odd level. That is, about incorporation and maintenance of the clocked inverters 1432 and 1436 of even level, it is equivalent to the thing of odd level, and the thing which interchanged, respectively.

[0042] In such a configuration, the output of a clocked inverter 1432 returns to the input of a clocked inverter 1436 while being outputted from this latch circuit 1430, after it is reversed with an inverter 1434. Consequently, while the clocked inverter 1432 of odd level incorporates an input signal in the standup of a clock signal CLX, the clocked inverter 1432 of the even level following this will incorporate an input signal in the standup of reversal clock signal CLXINV. Therefore, the signal P (i+1) outputted from the inverter 1434 of even level is equivalent to that for which only the half period of a clock signal CLX (reversal clock signal CLXINV) was delayed from the signal Pi outputted from the inverter 1434 of the preceding paragraph. That is, the signals P1-Pn outputted, respectively become that to which the clock signal CLX carried out the anti-period [every] sequential shift of the transfer initiation pulse DX inputted into the No. 1 beginning from the latch circuit 1430 of step [1st] - the n-th step. In addition, i is for generalizing and explaining the latch circuit 1430 of the 1st step - a ** (n+1) stage. Moreover, a latch circuit 1430 is an example of a unit circuit, in addition may use a flip-flop, a capacity circuit, etc., and may use them, combining these suitably.

[0043] Next, n logical circuit units U1-Un are explained. two which each logical circuit units U1-Un follow as shown in drawing 2 -- it corresponds latch circuit 1430, and is prepared respectively, and the sampling signals S1-Sn are generated based on the output signal of the latch circuit 1430 of the preceding paragraph, and the output signal of a latter latch circuit.

[0044] Each logical circuit units U1-Un are constituted from NAND circuit 1464, an inverter 1476, and NOR circuit 1474 by each. NAND circuit 1464 of the logical circuit unit Ui outputs as a signal Qi what reversed the AND of the output signal Pi of the i-th step of latch circuit 1430, and output-signal Pi+1 of the I+1st step of latch circuit 1430. If it puts in another way, the active period of Signal Qi is determined by NAND circuit 1474 based on Signal Pi and signal Pi+1. Here, if variation is in the property of TFT which constitutes latch circuit 1430 grade, the active period of Signals Q1-Qn may be overlapped mutually.

[0045] In order to abolish generating of this overlap, the logical circuit unit Ui is further equipped with the inverter 1476 and NOR circuit 1474. First, an inverter 1476 functions as a delay circuit which outputs that for which only predetermined time was delayed with the i-th step in output signal Pi+1 of the latch circuit of the latter part among the i+1st step of latch circuits 1430 corresponding to the logical circuit unit Ui as a signal Ri. Here, in the overlap period, tb, then the time delay td of an inverter 1476 are set up so that it may become long a little rather than tb.

[0046] Next, NOR circuit 1474 outputs reversal of the OR of Signal Qi and an inverter 1476 as a sampling signal Si. Here, if the propagation delay time of NAND circuit 1464 is disregarded, in accordance with the initiation timing of the active period of signal Pi+1, the termination timing of initiation timing of the active period of Signal Qi of the active period of Signal Qi corresponds with the termination timing of the active period of Signal Pi. On the other hand, only a time delay td delays signal Pi+1, and Signal Ri is reversed and acquired. Therefore, if the propagation delay time of NOR circuit 1474 is disregarded, while the initiation timing of the active period of the sampling signal Si is in agreement with the initiation timing of the active period of Signal Ri, the termination timing of the

active period of the sampling signal Si is in agreement with the termination timing of the active period of Signal Qi. That is, NOR circuit 1474 has the function to restrict the active period of Signal Qi, based on Signal Ri.

[0047] Therefore, each active period of the sampling signals S1-Sn outputted from each logical circuit units U1-Un is restricted so that it may become short to each active period of Signals Q1-Qn. Here, the time difference of the active period of Signal Qi and the active period of the sampling signal Si is given by the time delay td of an inverter 1476. Moreover, as mentioned above, since the time delay td is set up so that it may become long a little from the overlap period tb, it can lose the overlap of the sampling signals S1-Sn.

[0048] A <sampling circuit>, next the sampling circuit 150 in drawing 1 are explained. A sampling circuit 150 makes the six data lines 114 one group (block), to the data line 114 belonging to these groups, according to the sampling signals S1-Sn, samples picture signals VID1-VID6, respectively, and supplies them. A sampling circuit 150 becomes a detail from the switch 151 formed every data line 114, and each switch 151 has the composition that a sampling signal is supplied to the gate while being inserted between the end of the data line 114, and the signal line with which either of the picture signals VID1-VID6 is supplied. About the concrete configuration of a switch 151, you may constitute with a configuration with the N channel mold TFT shown in drawing 4 (a), a configuration with the P channel mold TFT shown in this drawing (b), or the complementary type TFT shown in this drawing (c), for example.

[0049] A <scanning-line drive circuit>, next the scanning-line drive circuit 130 are explained. As compared with the data-line drive circuit 140, as for the scanning-line drive circuit 130, the direction of a drawer and the signal inputted of an output signal differ from each other. Namely, as it is equivalent to what carried out the RLC of the data-line drive circuit 140 90 degrees, and has arranged it and is shown in drawing 1 , instead of the transfer initiation pulse DX, the scanning-line drive circuit 130 inputs Pulse DY, and has the composition of inputting a clock signal CLY and its reversal clock signal CLYINV, for every horizontal scanning period instead of a clock signal CLX and its reversal clock signal CLXINV.

[0050] Therefore, the latch circuit 1430 and n Logical unit U1-Un by which cascade connection was carried out to the stage (n+1) constitute like [circuit / 130 / concerning this operation gestalt / scanning-line drive] the data-line drive circuit 140 mentioned above. Although overlap may be mutually produced by this circuitry at the active period of the signal outputted from each latch circuit 1430, the active period of n signals S1-Sn outputted from each Logical unit U1-Un can be made not to produce overlap mutually. Therefore, if this signal is used as a scanning-line signal, the scanning line with which the same picture signals differ will not be supplied.

[0051] <Actuation of this operation gestalt>, next the actuation in the liquid crystal equipment concerning the configuration mentioned above are explained.

[0052] A sequential shift is carried out by a clock signal CLY and its reversal clock signal CLYINV, and the transfer initiation pulse DY supplied to the scanning-line drive circuit 130 is outputted to each scanning line 112. And two or more one data line 114 is chosen at a time as line sequential in the direction of Y.

[0053] Hereafter, with reference to the timing chart shown in drawing 5 and drawing 6 , it explains that the signal in the data-line drive circuit 140 flows. Drawing 5 is a timing chart which shows outline actuation of the data-line drive circuit 140.

[0054] As shown in this drawing, one picture signal Video is distributed to picture signals VID1-VID6 by the picture signal processing 300, and is elongated 6 times to a time-axis. Furthermore, in the beginning of the beginning of the period when a certain data line is chosen, i.e., a horizontal scanning period, the transfer initiation pulse DX is supplied to the data-line drive circuit 140.

[0055] According to a clock signal CLX and reversal clock signal CLXINV, the sequential output of the transfer initiation pulse DX supplied to the latch circuit 1430 of the first rank is carried out as signals P1-Pn from each latch circuit 1430. And the sequential output of the signals Q1-Qn is carried out from each NAND circuit 1464 prepared respectively corresponding to two continuous latch circuits 1430. Moreover, the sequential output of the signals R1-Rn with which only time amount td delayed Signals

P1-Pn is carried out by the inverter 1476 formed to the output terminal of each latch circuit 1430. Moreover, based on these signals R1-Rn and Signals Q1-Qn, NOR circuit 1474 carries out sequential generation of the sampling signals S1-Sn.

[0056] Drawing 6 is a timing chart which shows each wave of the signals P1-P4 mentioned above, signals Q1-Q3, signals R1-R3, and signals S1-S3. Here, variation shall be in Vth of the P channel mold TFT which constitutes a latch circuit 1430, NAND circuit 1464, and an inverter 1476, and the variation in other components shall be disregarded. Moreover, in this drawing, as for the field smeared away black, the generating timing of a rising edge or a falling edge shows the barrack range.

[0057] As shown in drawing, the timing of the rising edge of each signals P1-P4 outputted from the latch circuit 1430 of the 1st step to the 3rd step is generated in the field smeared away black according to variation to Vth of the P channel mold TFT which constitutes them. On the other hand, there is variation in Vth also in the P channel mold TFT of NAND circuit 1464. For this reason, as shown in drawing, an active period (L level) may overlap each output signals Q1-Q3 of NAND circuit 1464. For example, the active period of a signal Q1 expires in timing t38, and period overlap of the thing which the active period of a signal Q2 starts from timing t37, then a signal Q1 and a signal Q2 is carried out from timing t37 to t38.

[0058] Signals R1-R3 are signals which only time amount td made carry out delay reversal of the signals P2-P4 with an inverter 1476. As mentioned above, the time delay td of an inverter 1476 is set up so that it may become longer than the overlap period tb. For this reason, the initiation timing of the active period (L level) of signals R2 and R3 surely becomes behind from the termination timing of the active period (H level) of signals Q1 and Q2. For example, the thing by which a signal P3 changes from L level to H level in timing t37, then a signal R2 change from H level to L level, when time amount td has passed since timing t37 and it results in timing t39. The thing which the rising edge of a signal Q1 generates behind time on the other hand most by the variation in the Vth value of the P channel mold TFT which constitutes NAND circuit 1464, then the active period of a signal Q1 are ended to timing t38. That is, the initiation timing of the active period (L level) of a signal R2 surely becomes behind from the termination timing of the active period (H level) of a signal Q1.

[0059] Next, signals S1-S3 are generated by NOR circuit 1474 based on signals Q1-Q3 and signals R1-R3. The output signal of NOR circuit 1474 is given as an AND, although each input signal was reversed and carried out. Therefore, the active period (H level) of signals S1-S3 turns into a period when the active period (L level) of signals Q1-Q3 and the active period (L level) of signals R1-R3 overlap. Since only time amount td is delayed and signals R1-R3 are acquired in a signal P2 - a signal P4, the active period of signals S1-S3 becomes what restricted the active period of signals Q1-Q3 by the active period of signals R1-R3. Specifically, the initiation timing of the active period of signals Q1-Q3 is restricted by signals R1-R3.

[0060] For example, when its attention is paid to a signal S2, in the signal Q2 before being restricted, the initiation timing of an active period is in within the limits from timing t37 to t38. Since the initiation timing of an active period restricts this with the signal R2 in within the limits from timing t39 to t40, though the initiation timing of the active period of a signal S2 is the earliest, it turns into timing t39. On the other hand, though the termination timing of a signal S1 is the latest, it is timing t38. That is, the initiation timing of a signal S2 surely becomes behind from the termination timing of a signal S1. Therefore, it cannot happen that the active period of a signal S1 and a signal S2 overlaps. Thus, it cannot happen by setting the time delay td of an inverter 1476 as the thing [a little] longer than the variation period tb of a signal to overlap between other signals S1 - Sn at a mutual active period like the relation between a signal S1 and a signal S2.

[0061] In addition, this time delay td can be adjusted by transposing the configuration of a delay circuit 1474 to the inverter of 3 ream, and a delay line, or changing the gate size of an inverter. Since this adjustment can be performed per several ns, the active (H level) period between a signal S1 - Sn does not become narrowed beyond at the need, either.

[0062] The above signals S1-Sn are used as a sampling signal in the data drive circuit 140 concerning this operation gestalt. For example, when the sampling signal S1 serves as H level, picture signals

VID1-VID6 will be sampled by the six data lines 114 belonging to this group, respectively, and it will be written in six elements which intersect the scanning line with which these picture signals VID1-VID6 were chosen at present by TFT116 concerned, respectively. Then, if the sampling signal S2 serves as H level, picture signals VID1-VID6 will be shortly sampled by the following six data lines 114, respectively, and these picture signals VID1-VID6 will be written in six elements which intersect the scanning line 112 chosen at that time by TFT116 concerned, respectively. Since the active (H level) period of the sampling signal S1 and the sampling signal S2 does not overlap as mentioned above, the problem on which display grace is reduced is not produced, either.

[0063] Like the following, when the sampling signal S3, S4, ..., Sn serve as H level one by one, picture signals VID1-VID6 will be sampled by the six data lines 114 belonging to each sampling signal, respectively, and these picture signals will be written in six pixels which intersect the scanning line 112 chosen at the time, respectively. And after this, the following scanning line 112 is chosen, again, the sequential output of the sampling signals S1-Sn will be carried out, and the same writing will be performed repeatedly.

[0064] In addition, by such drive method, since the sampling time of the picture signal by each switch 151 becomes 6 times as compared with the method which drives the data line 114 for [every], the charge and discharge time in each pixel is fully secured. For this reason, high contrast-ization will be attained. Furthermore, the frequency of the number of stages of the latch circuit 1430 in the data-line drive circuit 140, a clock signal CLX, and its reversal clock CLXINV is reduced to one sixth, respectively, and reduction-izing and low-power-izing of a number of stages are also attained.

[0065] The whole liquid crystal panel 100 configuration which has <the example of a configuration of a liquid crystal panel>, next the data-line drive circuit 140 concerning each operation gestalt mentioned above is explained with reference to drawing 7 and drawing 8 . Here, drawing 7 is the perspective view showing the configuration of a liquid crystal panel 100, and drawing 8 is the sectional view of the A-A' line in drawing 7 .

[0066] The component substrates 101, such as glass with which, as for the liquid crystal panel 100, the pixel electrode 118 grade was formed, and a semi-conductor, a quartz, While lamination is carried out so that the transparent opposite substrates 102, such as glass with which the common electrode 108 grade was formed, may maintain fixed spacing by the sealant 104 in which the spacer 103 was mixed and an electrode forming face may counter mutually The structure where the liquid crystal 105 as an opto electronics material was enclosed with this spacing is taken. Although a sealant 104 is formed along the substrate circumference of the opposite substrate 102, in order to enclose liquid crystal 105, the part is carrying out opening of it. For this reason, the closure of that opening part is carried out with the sealing agent 106 after enclosure of liquid crystal 105.

[0067] Here, it is the opposed face of the component substrate 101, and in one side of external surface of a sealant 104, the data-line drive circuit 140 and sampling circuit 150 which were mentioned above are formed, and it has the composition of driving the data line 114 which extends in the direction of Y. Furthermore, two or more external circuit connection terminals 107 are formed in this one side, and it has the composition of inputting the various signals from a timing generator 200 and the picture signal processing circuit 300.

[0068] The electric flow with the component substrate 101 is achieved by the flow material in which the common electrode 108 of the opposite substrate 102 was formed in at least one place among four corners in a pasting part with the component substrate 101. Otherwise, the color filter arranged the shape of SUTORAIBU, the shape of the shape of MOBAIKU and a triangle, etc. to the 1st is prepared corresponding to the application of a liquid crystal panel 100, light-shielding films, such as resin black which distributed metallic materials, such as chromium and nickel, carbon, titanium, etc. to the 2nd at the photoresist, are prepared in the opposite substrate 102, and the back light which irradiates [3rd] light at a liquid crystal panel 100 is prepared in it. In addition, a light-shielding film is prepared in the opposite substrate 102, without forming a color filter in the case of the application of a colored light modulation.

[0069] Moreover, while the orientation film (illustration abbreviation) by which rubbing processing was

carried out is prepared in the predetermined direction, respectively, the polarizing plate (illustration abbreviation) according to the direction of orientation is prepared in the opposed face of the component substrate 101 and the opposite substrate 102 at each that tooth-back side, respectively. However, since efficiency for light utilization will increase as a result of the above-mentioned orientation film's, an above-mentioned deflecting plate's, etc. becoming unnecessary if the polymer dispersed liquid crystal distributed as a very small grain is used into a macromolecule as liquid crystal 105, in points, such as a raise in brightness, and low-power-izing, it is advantageous.

[0070] In addition, it is good also as a configuration connected electrically and mechanically through the anisotropy flow film in which IC chip for a drive mounted in the film using the TAB (Tape Automated Bonding) technique instead of forming some or all of a circumference circuit of drive circuit 120 grade in the component substrate 101 is prepared in the predetermined location of the component substrate 101. Moreover, it is good also as a configuration which connects the IC chip for a drive itself to the predetermined location of the component substrate 101 electrically and mechanically through an anisotropy flow film using a COG (Chip On Grass) technique.

[0071] In the <relation between number of conversion, and number of the data lines which constitutes one group> above-mentioned explanation a sampling circuit 150 Although it constitutes so that the picture signals VID1-VID6 changed into six lines may be sampled and supplied to coincidence to the six data lines 114 made into one group and picture signals VID1-VID6 may be impressed one by one for every data-line group The number of the data lines (namely, the number of the data lines which constitutes one group) impressed to this number of conversion and coincidence is not restricted to "6." For example, as long as the speed of response of the switch 151 in a sampling circuit 150 is fully high, you may constitute so that a serial transmission may be carried out to one signal line, without changing a picture signal into parallel and a sequential sampling may be carried out every data line 114. Moreover, it is good also as a configuration which three-line conversion, 12-line conversion, 24-line conversion, etc. carry out [as opposed to / as "3", "12", "24", etc. / the data lines such as 3, 12, and 24,] the number of the data lines impressed to the number of conversion, and coincidence, and supplies the picture signal which carried out juxtaposition supply to coincidence. In addition, it is desirable when that it is the multiple of 3 simplifies control, a circuit, etc. from the relation of the picture signal of a color consisting of a signal concerning three primary colors as the number of the data lines impressed to the number of conversion, and coincidence.

[0072] In the configuration of a component substrate, etc. and <operation> gestalten [which was mentioned above] While transparent insulating substrates, such as glass, constitute the component substrate 101 of a liquid crystal panel 100 and forming a silicon thin film on the substrate concerned Although TFT by which the source, the drain, and the mold were formed on the thin film concerned explained as what constitutes the switching element (TFT116) of a pixel, and the component of the drive circuit 120, this invention is not restricted to this.

[0073] For example, a semi-conductor substrate may constitute the component substrate 101, and the insulated gate field effect transistor by which the source, the drain, and the mold were formed in the front face of the semi-conductor substrate concerned may constitute the switching element of a pixel, and the component of the drive circuit 120. Thus, since it cannot use as an electro-optic device of a transparency mold when a semi-conductor substrate constitutes the component substrate 101, the pixel electrode 118 will be formed with aluminum etc. and it will be used as a reflective mold. Moreover, it is only good also considering the pixel electrode 118 as a reflective mold, using the component substrate 101 as a transparency substrate.

[0074] Furthermore, although the switching element of a pixel was explained as a 3 terminal component represented with TFT if it was in the gestalt of operation mentioned above, you may constitute from 2 terminal components, such as diode. However, in using 2 terminal component as a switching element of a pixel, while forming the scanning line 112 in one substrate and forming the data line 114 in the substrate of another side, it is necessary to form 2 terminal component between either the scanning line 112 or the data line 114 and a pixel electrode. In this case, a pixel will consist of a pixel electrode to which 2 terminal component is connected, a signal line (the data line 114 or the scanning line 112 on the

other hand) formed in an opposite substrate, and liquid crystal pinched among these.
[0075] Furthermore, as an opto electronics material, an electroluminescent element etc. can be used other than liquid crystal, and it can apply also to the display which displays according to the electro-optical effect. That is, this invention is applicable to all the electro-optic devices that have a configuration similar to the liquid crystal equipment mentioned above.
[0076] Although the pixel electrode 118 connected to one TFT116 and this was formed, this invention is not limited to this, and prepares two or more TFT(s) in 1 pixel as a switching element, and you may make it give a memory function to each pixel in <the configuration of a pixel>, and the operation gestalt mentioned above in the pixel corresponding to each intersection of two or more scanning lines 112 and two or more data lines 114. In short, if a switching element and a pixel electrode are prepared corresponding to the crossover of the scanning line and the data line, it is sufficient, and the number of the switching element per pixel does not ask.
[0077] The case where <electronic equipment>, next the liquid crystal equipment mentioned above are applied by various kinds of electronic equipment is explained. In this case, electronic equipment is mainly constituted by the source 1000 of a display information output, the display information processing circuit 1002, a power circuit 1004, a liquid crystal panel 100, the drive circuit 120, and the timing generator 200, as shown in drawing 9 . In addition, the drive circuit 120 is built in the liquid crystal panel 100. Among these, the source 1000 of a display information output is equipped with the tuning circuit which carries out the alignment output of storage units, such as ROM (Read Only Memory), and memory, such as RAM (Random Access Memory), various disks, and the picture signal, and supplies display information, such as a picture signal of a predetermined format, to the display information processing circuit 1002 based on various kinds of clock signals generated by the timing generator 200. Next, the display information processing circuit 1002 is equipped with various well-known circuits, such as the S/P conversion circuit 302 mentioned above, and a rotation circuit besides magnification and an inverter circuit 304, a gamma correction circuit, a clamping circuit, performs processing of display information in which it inputted, and supplies the picture signal to the drive circuit 120 with a clock signal CLX. In addition, in drawing 13 , although the clock signal CLX is supplied through the display information processing circuit 1002, as shown in drawing 1 , it is good also as a configuration in which the drive circuit 120 is supplied directly and the display information processing circuit 1002 which is the high order configuration of the image-processing circuit 300 operates from a timing generator 200 synchronizing with the clock signal by the timing generator 200.
[0078] Next, some of examples which used for the concrete electronic circuitry the liquid crystal panel 100 mentioned above are explained.
[0079] < -- that projector that used this liquid crystal panel as a light valve at the beginning of 1:projector > is explained. Drawing 10 is the top view showing the configuration of this projector. As shown in this drawing, the lamp unit 1102 which consists of sources of the white light, such as a halogen lamp, is formed in the projector 1100 interior. It is separated into the three primary colors of RGB by the mirror 1106 of three sheets and the dichroic mirror 1108 of two sheets which have been arranged inside, and the incident light injected from this lamp unit 1102 is led to the liquid crystal panels 100R, 100B, and 100G as a light valve corresponding to each primary color, respectively. Here, the light of B color is drawn through the relay lens system 1121 which consists of the incidence lens 1122, a relay lens 1123, and an outgoing radiation lens 1124, in order to prevent the loss, since the optical path is long as compared with other R colors and G colors.
[0080] It drives, respectively with the primary signal of R, G, and B which are equivalent to the liquid crystal panel 100 mentioned above as for the configuration of liquid crystal panels 100R, 100B, and 100G, and are supplied from a picture signal processing circuit (illustration abbreviation). And incidence of the light modulated with these liquid crystal panels is carried out to a dichroic prism 1112 from three directions. In this dichroic prism 1112, while the light of R color and B color is refracted at 90 degrees, the light of G color goes straight on. Therefore, as a result of compounding the image of each color, it will be projected on a color picture by the screen 1120 through a projector lens 1114.
[0081] When its attention is paid here about the display image by each liquid crystal panels 100R, 100B,

and 100G, it is necessary for the display image by liquid crystal panel 100G to carry out right-and-left reversal to the display image by each liquid crystal panels 100R and 100B. For this reason, the direction of a horizontal scanning serves as relation of hard flow mutually with liquid crystal panel 100G and liquid crystal panels 100R and 100B. In addition, since it is projected on the light corresponding to each primary color of R, G, and B by liquid crystal panels 100R, 100B, and 100G with a dichroic mirror 1108, it is not necessary in them to prepare a color filter.

[0082] The example which applied <that 2:mobile mold computer>, next this liquid crystal panel to the personal computer of a mobile mold is explained. Drawing 11 is the perspective view showing the configuration of this personal computer. In drawing, the computer 1200 consists of the body section 1204 equipped with the keyboard 1202, and a liquid crystal display unit 1206. This liquid crystal display unit 1206 is constituted by adding a back light to the tooth back of the liquid crystal panel 100 described previously.

[0083] < -- that 3:cellular-phone > -- the example which applied this liquid crystal panel to the cellular phone is explained further. Drawing 12 is the perspective view showing the configuration of this cellular phone. In drawing, a cellular phone 1300 is equipped with a liquid crystal panel 100 with the ear piece 1304 besides two or more manual operation buttons 1302, and a speaker 1306. A back light is prepared in the tooth back also at the liquid crystal panel 100 if needed.

[0084] In addition, **, such as a device which it explained with reference to drawing 10 - drawing 12 as electronic equipment, and also was equipped with the video tape recorder of a liquid crystal television, and a viewfinder mold and a monitor direct viewing type, car navigation equipment, a pager, an electronic notebook, a calculator, a word processor, the workstation, the TV phone, the POS terminal, and the touch panel, are mentioned. And an electro-optic device is applicable to the liquid crystal panel of each operation gestalt, and a pan to those various electronic equipment.

[0085]

[Effect of the Invention] Since generating of the overlap period of the sampling signal outputted from a data-line drive circuit or the signal outputted from a scanning-line drive circuit is beforehand prevented according to this invention as explained above, it becomes possible to suppress deterioration of display grace. For this reason, it is not necessary to supply an external signal.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] It is the drive circuit of the electro-optic device which has the switching element prepared corresponding to the crossover with two or more scanning lines, two or more data lines, and said each scanning line and said each data line, and a pixel electrode. Two or more unit circuits which carry out a sequential shift and output an input signal according to a clock signal, Corresponding to two continuous unit circuits, it is prepared respectively, and has two or more unit drive circuits which generate the signal which chooses said each scanning line or said each data line. Said unit drive circuit The delay circuit which delays a latter output signal between two corresponding unit circuits, it is inputted into this unit drive circuit -- this -- the drive circuit of the electro-optic device characterized by providing the limiting circuit which restricts the active period determined by the output signal of two unit circuits based on the output signal of said delay circuit.
[Claim 2] Said limiting circuit is a drive circuit of the electro-optic device according to claim 1 characterized by restricting the initiation timing of said active period based on the output signal of said delay circuit.
[Claim 3] It is the drive circuit of the electro-optic device according to claim 2 which constitutes said delay circuit from an inverter and is characterized by equipping said limiting circuit with the NAND circuit which inputs the output signal of two continuous unit circuits, and the NOR circuit which restricts the active period of the output signal of this NAND circuit with the output signal of said inverter.
[Claim 4] The switching element connected to the scanning line, two or more data lines, and two or more of said each scanning line and said each data line, Two or more unit circuits which are data-line drive circuits of the electro-optic device which has the pixel electrode connected to said switching element, carry out a sequential shift and output an input signal according to a clock signal, Two or more unit drive circuits which generate the sampling signal which is respectively established corresponding to two continuous unit circuits, and chooses said each data line, It has two or more switches which sample a picture signal based on said sampling signal, and are supplied to said data line. Said unit drive circuit The delay circuit which delays a latter output signal between two corresponding unit circuits, it is inputted into this unit drive circuit -- this -- the data-line drive circuit of the electro-optic device characterized by providing the limiting circuit which restricts the active period determined by the output signal of two unit circuits based on the output signal of said delay circuit.
[Claim 5] Two or more switches corresponding to said each data line are the data-line drive circuits of the electro-optic device according to claim 4 characterized by the thing which it blocks [things] corresponding to said data line of m (m is the two or more natural numbers) book, and had said sampling signal blocked, and to supply for every switch.
[Claim 6] It is the scanning-line drive circuit of the electro-optic device which has two or more switching elements prepared by carrying out crossover correspondence and pixel electrodes of the scanning line, two or more data lines, and said each scanning line and said each data line. Two or more unit circuits which carry out a sequential shift and output an input signal according to a clock signal,

Corresponding to two continuous unit circuits, it is prepared respectively, and has two or more unit drive circuits which generate the signal which chooses said each scanning line. Said unit drive circuit The delay circuit which delays a latter output signal between two corresponding unit circuits, it is inputted into this unit drive circuit -- this -- the scanning-line drive circuit of the electro-optic device characterized by providing the limiting circuit which restricts the active period determined by the output signal of two unit circuits based on the output signal of said delay circuit.

[Claim 7] It is the electro-optic device which said image display field consists of substrates of the pair which carries out phase opposite, and is characterized by having the transistor opened and closed according to the scan signal supplied to said scanning line while being an electro-optic device equipped with the drive circuit and image display field of an electro-optic device according to claim 1 and being inserted between the pixel electrode arranged in the shape of a matrix at one substrate, said pixel electrode, and said data line.

[Claim 8] Electronic equipment characterized by using an electro-optic device according to claim 7 for a display.

[Translation done.]

ュータに適用した例について説明する。図11は、このパーソナルコンピュータの構成を示す斜視図である。図において、コンピュータ1200は、キーボード1202を備えた本体部1204と、液晶表示ユニット1206とから構成されている。この液晶表示ユニット1206は、先に述べた液晶パネル100の背面にバックライトを付加することにより構成されている。

【0083】<その3：携帯電話>さらに、この液晶パネルを、携帯電話に適用した例について説明する。図12は、この携帯電話の構成を示す斜視図である。図において、携帯電話1300は、複数の操作ボタン1302のほか、受話口1304、送話口1306とともに、液晶パネル100を備えるものである。その液晶パネル100にも、必要に応じてその背面にバックライトが設けられる。

【0084】なお、電子機器としては、図10～図12を参照して説明した他にも、液晶テレビや、ビューファインダ型、モニタ直視型のビデオテープレコーダ、カーナビゲーション装置、ページャ、電子手帳、電卓、ワードプロセッサ、ワークステーション、テレビ電話、POS端末、タッチパネルを備えた機器等等が挙げられる。そして、それらの各種電子機器に対して、各実施形態の液晶パネル、さらには電気光学装置が適用可能である。

【0085】

【発明の効果】以上説明したように本発明によれば、データ線駆動回路から出力されるサンプリング信号や走査線駆動回路から出力される信号のオーバーラップ期間の発生が未然に防止されるため、表示品位の低下を抑えることが可能となる。このために外部信号を供給する必要もない。

【図面の簡単な説明】

【図1】　本発明の実施形態に係る駆動回路を適用した液晶装置の全体構成を示すブロック図である。

【図2】　同液晶装置におけるデータ線駆動回路の構成を示すブロック図である。

【図3】　同データ線駆動回路のラッチ回路の構成例を示す回路図である。

【図4】　（a）～（c）は、それぞれ同液晶装置におけるサンプリング回路のスイッチ構成を示す回路図である。

【図5】　同データ線駆動回路の動作を説明するためのタイミングチャートである。

【図6】　同データ線駆動回路の動作を説明するためのタイミングチャートである。

【図7】　同液晶パネルの構造を示す斜視図である。

【図8】　同液晶パネルの構造を説明するための一部断面図である。

【図9】　同液晶装置が適用される電子機器の概略構成を示すブロック図である。

【図10】　同液晶装置を適用した電子機器の一例たるプロジェクタの構成を示す斜視図である。

【図11】　同液晶装置を適用した電子機器の一例たるパーソナルコンピュータの構成を示す斜視図である。

【図12】　同液晶装置を適用した電子機器の一例たる携帯電話の構成を示す斜視図である。

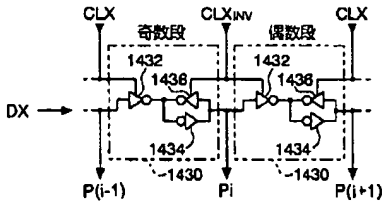
【図13】　従来技術におけるデータ線駆動回路の構成を示すブロック図である。

【図14】　同データ線駆動回路の動作を説明するためのタイミングチャートである。

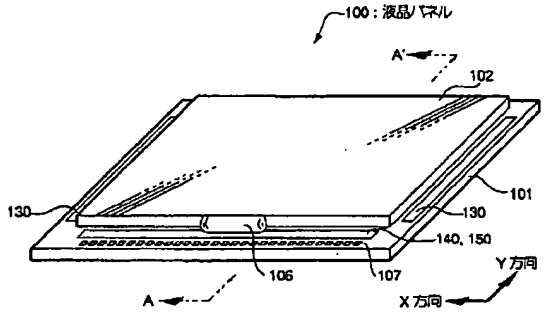
【符号の説明】

100……液晶パネル
101……素子基板
102……対向基板
116……TFT
120……駆動回路
130……走査線駆動回路
140……データ線駆動回路
150……サンプリング回路
151……スイッチ
1430……ラッチ回路
1464……NAND回路
1474……NOR回路
1476……NOT回路
1486……アナログスイッチ

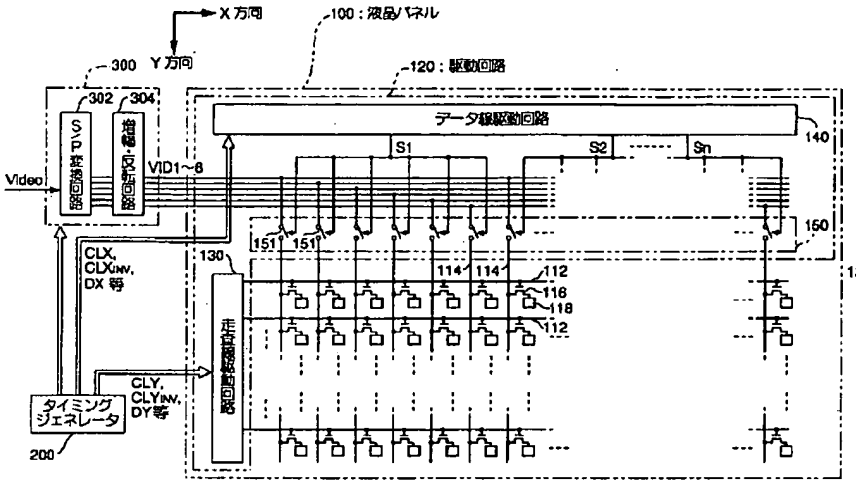
【図3】



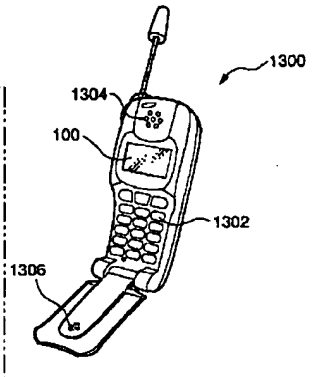
【図7】



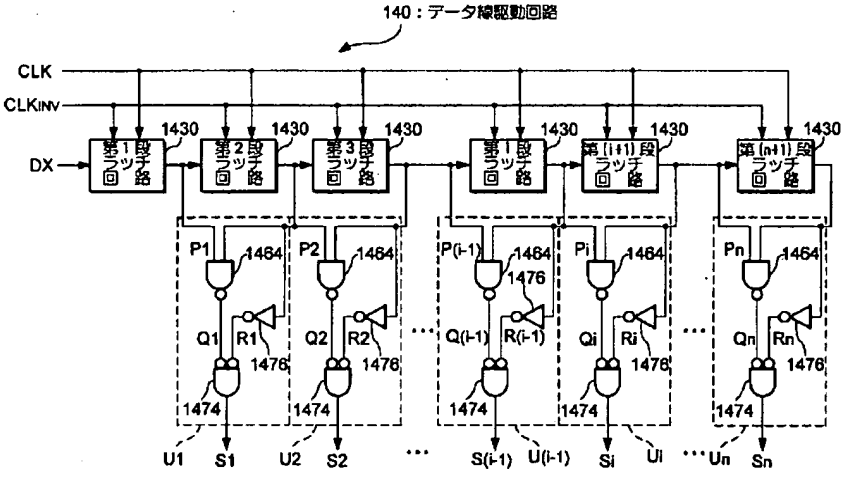
【図1】



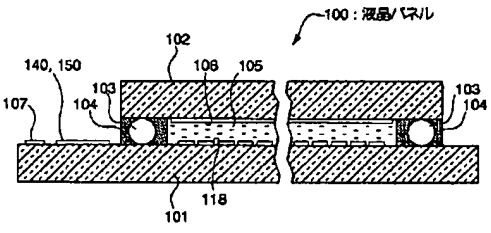
【図12】



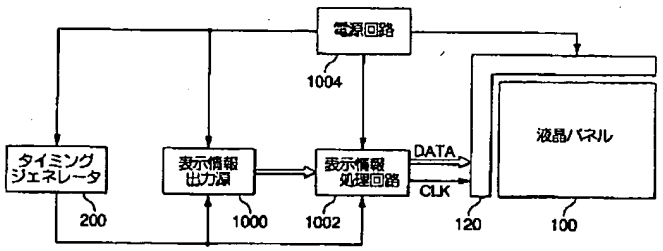
【図2】



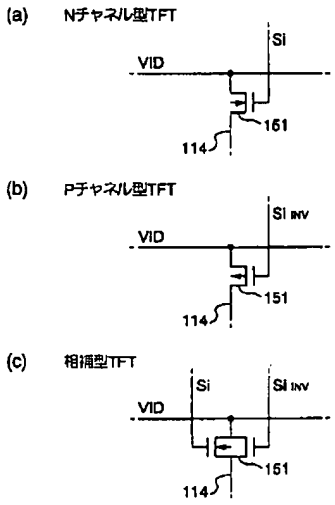
【図8】



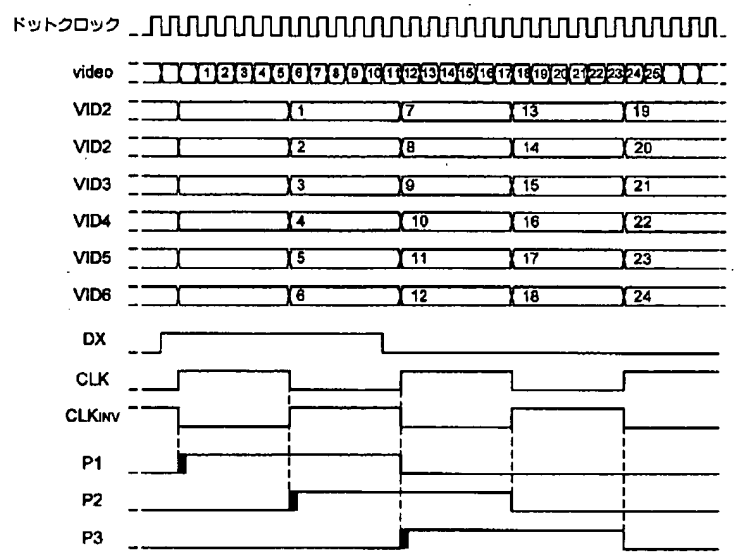
【図9】



【図4】



【図5】



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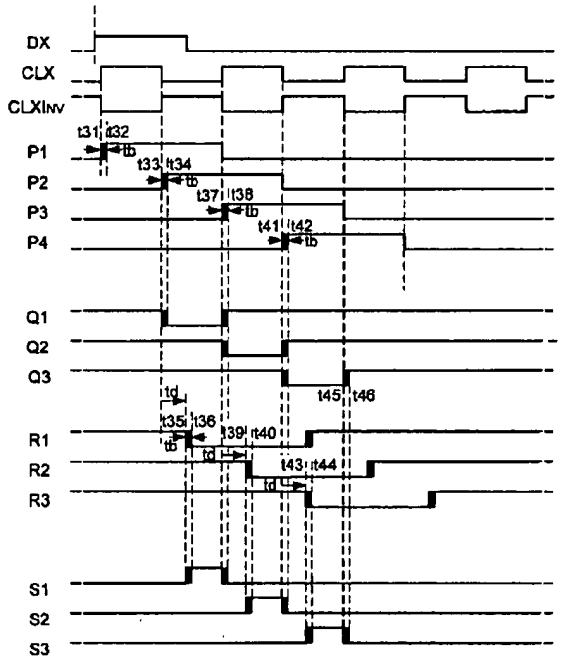

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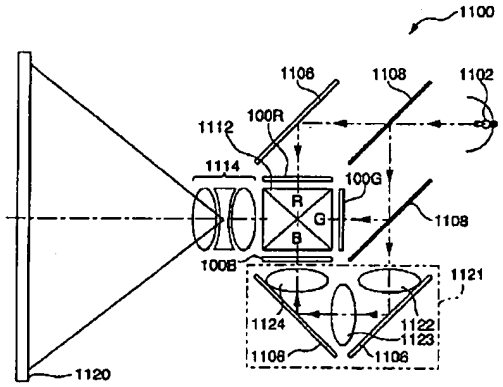

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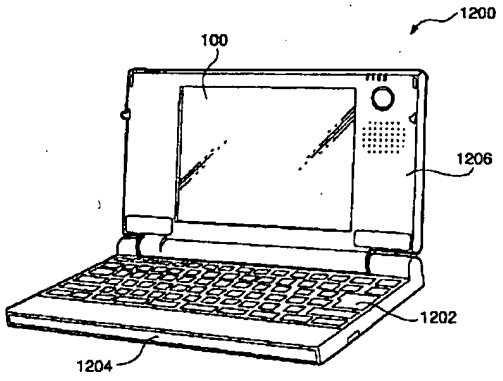

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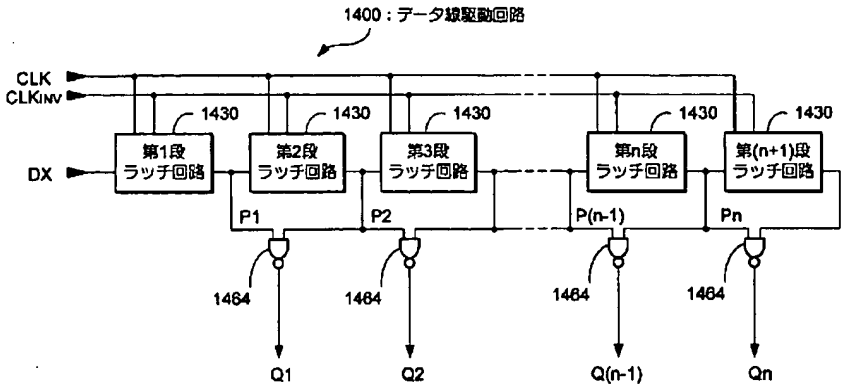

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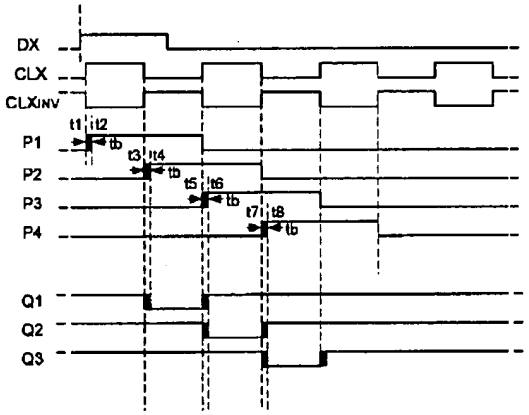

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Fターム(参考)　2H093 NA16 NC16 NC21 NC26 NC34
NC49 ND33 ND60 NG01 NG02
5C006 AA22 AF50 AF71 BB16 BC03
BC12 BF03 BF04 BF07 BF11
BF24 BF25 BF26 BF27 BF31
EC11 FA20 FA21
5C080 AA10 BB05 DD03 DD28 FF11
JJ02 JJ04 JJ06 KK07